Kadi Sarva Vishwavidyalaya, Gandhinagar

MASTERS OF COMPUTER APPLICATION (MCA)
Semester – I (First Year)
Subject: MCA-105 – Computer system Architecture (CSA)

SUB Total CREDIT	Teaching scheme (per week)		Examination scheme				
			MID	CEC	External		Total Marks
	Th.	Pr.	Th.	Th.	Th.	Pr.	
4	3	2	25	25	50	25	125

Course Description:
This course covers the design and architecture of computer and digital systems. It explains how bit information is processed in logical gates and how register array called memory is composed of these gates. It also avails knowledge of the internal structure and operation of a digital computer at the level of memory, registers, Processor and flow of control.

Objectives:
1. For students this course unveils the mystery behind the black box called computer. This is their first opportunity to see the control aspects of the machine and thus fully appreciate the entire system.
2. Students will able to explain different data representation (e.g., different number systems, 2's complement arithmetic, etc.) and design combinational/sequential circuits using different gates and flip-flops.

Prerequisites: None

Course Contents:

UNIT – I: Number System and Codes [20%]

Introduction, Radix Notation: Decimal, Binary, Octal and Hexadecimal, Conversion of Numbers from one radix form to another, Signed Binary Number, Floating Point Representation of Number, Binary Arithmetic: Addition, Subtraction, Multiplication and Division, Complement Binary Arithmetic: 1's Complement Arithmetic and 2's Complement Arithmetic, Arithmetic Overflow, Codes: BCD Code, 2-4-2-1 code, Excess 3 code, Gray code, Error Detecting Code: Parity codes, Error Correcting Code: Hamming Code

UNIT – II: Boolean Algebra and Logic Gates [20%]

Introduction, Boolean Algebra, Overview of Logic Circuit, De-Morgan's Theorems, Standard Representation for Logical Functions, Minterm and Maxterm, Simplification of Boolean Expressions: Algebraic simplification and Karnaugh Map: Simplification of Sum of Products and Simplification of Product of Sums, Don't Care condition

UNIT – III: Combinational Logic Circuits **[20%]**

Construction of the ALU, Binary Half-Adder, Full-Adder, Parallel Binary Adder, Binary-Coded-Decimal Adder, Binary Multiplication and Binary Division, Multiplexer, Demultiplexer

UNIT – IV: Sequential Logic Circuits **[20%]**

Flip-Flops, Transfer Circuits, Clocks, Flip-flop Designs, Gated Flip-flop, Master-Slave Flip-flop, Shift Register, Binary Counter: Ripple counter, gated-clocked binary counter and binary up-down counter, BCD Counter, Counter Design: Using RS Flip-flop and Using JK Flip-flop, Flip Flop Excitation Tables

UNIT – V: Semiconductor Memory Devices and Processor **[20%]**

Introduction, Memory Organization, Functional Diagram of Memory, Memory Operations, Characteristics of Memory Devices, Read and Write Memory, Read Only Memory, Central Processing Unit: CPU Organization, Instruction, Addressing Modes, Interrupts and Exceptions, Instruction Cycle, Instruction and Data Flow

Text Book(s):

1. Digital Electronics By G.K. Kharate, Oxford University Press
2. Digital Computer Fundamentals By Thomas C. Bartee, Sixth Edition Tata McGraw Hill
3. Computer Fundamentals: Architecture & Organization 4th Edition, B.Ram, New Age International Publishers

Other Reference Books:

1. Computer System Architecture By – Morris Mano,3rd Edition Prentice Hall of India
2. Computer Architecture and Organization By - B. Govindrajalu
3. Fundamentals of Digital Circuits By A. Anand Kumar, PHI publications
4. Computer Organization and Architecture By William Stallings, 6th edition, PHI

Practical List: (Practicals on LOGISIM simulation open source software environment)

1. Develop circuits of all the Gates.
2. Develop circuits of adder, subtractor, multiplier and divider.
3. Develop circuits of plexers – multiplexer, demultiplexer, & decoder.
4. Develop circuits of flip flops – RS Flip flop, JK Flip Flop & D Flip Flop.
5. Develop circuits of Shif register and Counter.