Kadi Sarva Vishwavidyalaya

Gandhinagar-382 015

B.E Semester: 7
Electronics & Communication Engineering
Subject Name: CMOS Analog Circuit Design
Subject Code: EC-704-D (EP 1)

A. Course Objective:

The educational objectives of this course are

- To present an introductory knowledge of analog IC design.
- To address the underlying concepts of different analog IC Design.

B. Teaching / Examination Scheme

SUBJECT		Teaching Scheme				Total Credit	Evaluation Scheme					Total Marks
		L	T	P	Total		THEORY		IE	CIA	PR. / VIVO	
CODE	NAME	Hrs	Hrs	Hrs	Hrs		Hrs	Marks	Marks	Marks	Marks	
EC- 704-D	CMOS Analog circuit Design	4	0	2	6	5	3	70	30	20	30	150

C. Syllabus

1 **Amplifiers:** Gate-Drain connected loads: Common source and common gate amplifiers, the source follower, Current source load: The cascode connection and the Push pull amplifier, Noise and Distortion in Amplifiers: Modeling Amplifier noise, Class AB amplifier, feedback amplifier

2 **Differential & Operational amplifiers:** The Source coupled pair: Current source load, CMRR, noise, matching, Source cross coupled pair: current source load,Cascode loads, Basic CMOS Opamp design

3 **Digital phase locked loop:** The phase detector, Voltage controlled oscillator **,**Loop filter

4 **Current sources and sinks &References:** The current mirror: Cascode connection, transient response, matching in MOSFET mirrors**,** Wilson current mirror

5 **Memory circuits:** RAM memory cell, DRAM and SRAM cells, Sense amplifier, Row/ column decoder

6 **Schmitt trigger:** Design, Switching characteristics **,**Applications.,Monostable and Astable Multivibrators .

7 **Non linear analog &Dynamic circuits:** Basic CMOS comparator design, Adaptive biasing**,** Analog multipliers, Level shifting

8 **Data Converters(ADC & DAC architecture):** Digital Input code resistor string,R-2R ladder

network current steering, Charge scaling and pipeline DAC, Two step flash ADC, pipeline ADC,Integrating ADC,Successive Approximation ADC

D. **Lesson Planning**

Sr. No.	No. of Hrs.	% Weight-age in Exam	Topic
1	11	20	**Amplifiers:** Gate-Drain connected loads: Common source and common gate amplifiers, the source follower, Current source load: The cascode connection and the Push pull amplifier, Noise and Distortion in Amplifiers: Modeling Amplifier noise, Class AB amplifier, feedback amplifier
2	10	15	**Differential & Operational amplifiers:** The Source coupled pair: Current source load, CMRR, noise, matching, Source cross coupled pair: current source load,Cascode loads, Basic CMOS Opamp design
3	05	10	**Digital phase locked loop:** The phase detector, Voltage controlled oscillator **,**Loop filter
4	06	10	**Current sources and sinks &References:** The current mirror: Cascode connection, transient response, matching in MOSFET mirrors**,** Wilson current mirror
5	0 6	10	**Memory circuits:** RAM memory cell, DRAM and SRAM cells, Sense amplifier, Row/ column decoder
6	06	10	**Schmitt trigger:** Design, Switching characteristics **,**Applications.,Monostable and Astable Multivibrators
7	06	10	**Non linear analog &Dynamic circuits:** Basic CMOS comparator design, Adaptive biasing**,** Analog multipliers, Level shifting
8	10	15	**Data Converters(ADC & DAC architecture):** Digital Input code resistor string,R-2R ladder network current steering, Charge scaling and pipeline DAC, Two step flash ADC, pipeline ADC, Integrating ADC, Successive Approximation ADC
TOTAL	60	100	

E. **Instructional Method & Pedagogy**

- At the start of course, the course delivery pattern , prerequisite of the subject will be discussed
- Lecture may be conducted with the aid of multi-media projector, black board, OHP etc. & equal weight age should be given to all topics while teaching and conduction of all examinations.
- Attendance is compulsory in lectures and laboratory, which may carries five marks in overall evaluation.
- One/Two internal exams may be conducted and total/average/best of the same may be converted to equivalent of 30 marks as a part of internal theory evaluation.
- Assignment based on course content will be given to the student for each unit/topic and will be evaluated at regular interval. It may carry an importance of ten marks in the overall internal evaluation.
- Surprise tests/Quizzes/Seminar/Tutorial may be conducted and having share of five marks in the overall internal evaluation.
- Experiments shall be performed in the laboratory related to course contents.

Suggested list of Experiments

Sr. No	Name Of Experiment
1	Evaluate I/V characteristic of MOS transistor using spice.
2	Evaluate on resistance of MOS switch using spice.
3	Design and Compare the specifications of various topologies of Single stage Amplifiers using 1micron Technology model parameters
4	Design and compare the performance of CMOS Current Mirrors using 1micron Technology model parameters
5	Design and evaluate the performance of a Simple CMOS Differential amplifiers using 1micron Technology model parameters

6	Design and compare the performance of different Voltage references using 1micron Technology model parameters
7	Design and verify the specifications of CMOS operational Amplifier using 1micron Technology
8	Design and simulate CMOS two stage op-amp using 1micron Technology model parameters
9	Design and simulate CMOS Comparator using 1micron Technology model parameters
10	Design and simulate CMOS Current conveyor using 1micron Technology model parameters
11	Design and simulate Low voltage operational amplifier using 1micron Technology model parameters

F. **Students Learning Outcomes**

On successful completion of the course, students can understand designing of analog IC. They are aware of different analog ICs which are used in many Industrial applications.

G. **Recommended Study Materials**

Text/ Reference Books:

1. CMOS Analog circuit Design, second edition ,Philip E.Allen,Douglas R.Holberg,Oxford Press
2. R. J. Baker, H. W. Li and D. E. Boyce, "CMOS: Circuit Design, Layout and Simulation", IEEE Press, 1998. (Cheap Edition).
3. B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2001. (Cheap Edition).