KADI SARVA VISHWAVIDYALAYA

B.E. Semester: V
Electronics & Communication Engineering
Subject Name: VLSI Technology and Design
Sub Code: EC-506 **W.E.F 2014-15**

A. Course Objective

The educational objectives of this course are

- Fundamentals of CMOS Digital VLSI design. Different Aspects of MOS inverters.
- MOS Logic circuits like combinational, sequential logic and dynamic logic circuits.
- FPGA & CPLD,VLSI Softwares: Xilinx, Quartus-II, Simulation tool : ModelSim.

B. Teaching / Examination Scheme:

SUBJECT		Teaching Scheme				Total Credit	Evaluation Scheme					Total Marks
		L	T	P	Total		THEORY		IE	CIA	PR. / VIVO	
CODE	NAME	Hrs	Hrs	Hrs	Hrs		Hrs	Marks	Marks	Marks	Marks	
EC-506	**VLSI Technology and Design**	**4**	**0**	**2**	**6**	**5**	**3**	**70**	**30**	**20**	**30**	**150**

C. Detailed Syllabus:

1 **Introduction**:
Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, computer aided design technology.

2 **Fabrication of MOSFET** :
Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.

3 **MOS Transistor** :
The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current- Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances

4 **MOS Inverters: Static Characteristics**:
Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement and Depletion type MOSFET load), CMOS Inverter

5 **Combinational MOS Logic Circuits** :
Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs).

6 **Sequential MOS Logic Circuits** :
Introduction, Behaviour of Bistable elements, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop.

7 **ASIC Design** :
Introduction, Design Methodologies, Introduction to Hardware Description Language (HDL): Structural, Behavioral, Data flow modeling, Concurrent and sequential VHDL, Test Benches, Finite State Machines

8 **Programmable Logic Devices** :
Basics of Programmable Logic Devices, Architectures of CPLD & FPGA, Design and Implementation using CPLD and FPGA.

D. Lesson Planning

Sr. No.	Lectures (Hours)	Weightage in % in Exam	Topics
1.	05	10	**Introduction**: Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, computer aided design technology
2.	05	10	**Fabrication of MOSFET :** Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.
3.	15	20	**MOS Transistor:** The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current- Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances
4.	05	10	**MOS Inverters: Static Characteristics:** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement and Depletion type MOSFET load), CMOS Inverter
5.	05	10	**Combinational MOS Logic Circuits** : Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs).
6.	05	10	**Sequential MOS Logic Circuits** : Introduction, Behaviour of Bistable elements, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered.
7.	15	20	**ASIC Design** : Introduction, Design Methodologies, Introduction to Hardware Description Language (HDL): Structural, Behavioral, Data flow modeling, Concurrent and sequential VHDL, Test Benches, Finite State Machines
8.	05	10	**Programmable Logic Devices** : Basics of Programmable Logic Devices, Architectures of CPLD & FPGA, Design and Implementation using CPLD and FPGA.
Total	60	100	

E Instructional Method And Pedagogy (ANNEXURE-I)

F Suggested List Of Experiments:

- All Practicals Based on VHDL/Verilog and Pspice/spice of MOSFET Characteristics

1. Introduction to programmable devices (FPGA, CPLD), Hardware Description Language (VHDL), and the use programming tool.

2. Implementation of basic logic gates and its testing.

3. Implementation of adder circuits and its testing.

4. Implementation of subtractor circuits and its testing.

5. Implementation 8 to 1 multiplexer and its testing.

6. Implementation of 3 to 8 decoder and its testing.

7. Implementation of J-K and D Flip Flops and its testing.

8. Implementation of sequential adder and its testing.

9. Implementation of BCD counter and its testing.

10. Implementation of two 8-bit multiplier circuits and its testing.

11. Implementation of any digital circuits using FSM.

12. Simulation of CMOS Inverter using SPICE for transfer characteristic.

13. Simulation and verification of two input CMOS NOR gate using SPICE.

14. VHDL/Verilog HDL based mini project

G. Students Learning Outcomes

On successful completion of the course:
The student can learn about detailed aspects to able design a digital VLSI system, to design different MOS logical circuits and to design digital parts using different VLSI software and implement on FPGA as well as CPLD, ASIC Design Flow.

H. Recommended Study Materials:

TEXT BOOKS:

1. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf Leblebici, TATA McGraw-Hill Pub. Company Ltd., Third Edition.
2. J. Bhasker, BHDL, Primer, Pearson Education Asia, Low Price Edition.
3. Xilinx and Altera Application Notes on the architecture of FPGAs and CPLDs.

REFERENCE BOOKS:

1. Basic VLSI Design By Pucknell and Eshraghian, PHI, 3rd ed.
2. D.Perry, BHDL, 2nd Ed., McGraw Hill International.
3. Introduction to VLSI Systems by Mead C and Conway, Addison Wesley
4. Introduction to VLSI Circuits & Systems – John P. Uyemura
5. Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic